ABSTRACT

A phase adjustment circuit generates multiple clock signals by, for example, successively delaying a first clock signal. One of the generated clock signals is selected and output. A phase difference detector determines whether the phase of the selected clock signal and the phase of a second clock signal satisfy a given condition. The clock signal selection can changed until the condition is satisfied, either by external control by a device that monitors a signal output by the phase difference detector, or by a built-in selection signal generator. This scheme assures that two clock signals with phases satisfying the given condition are obtained, regardless of environmental factors or fabrication variations.